

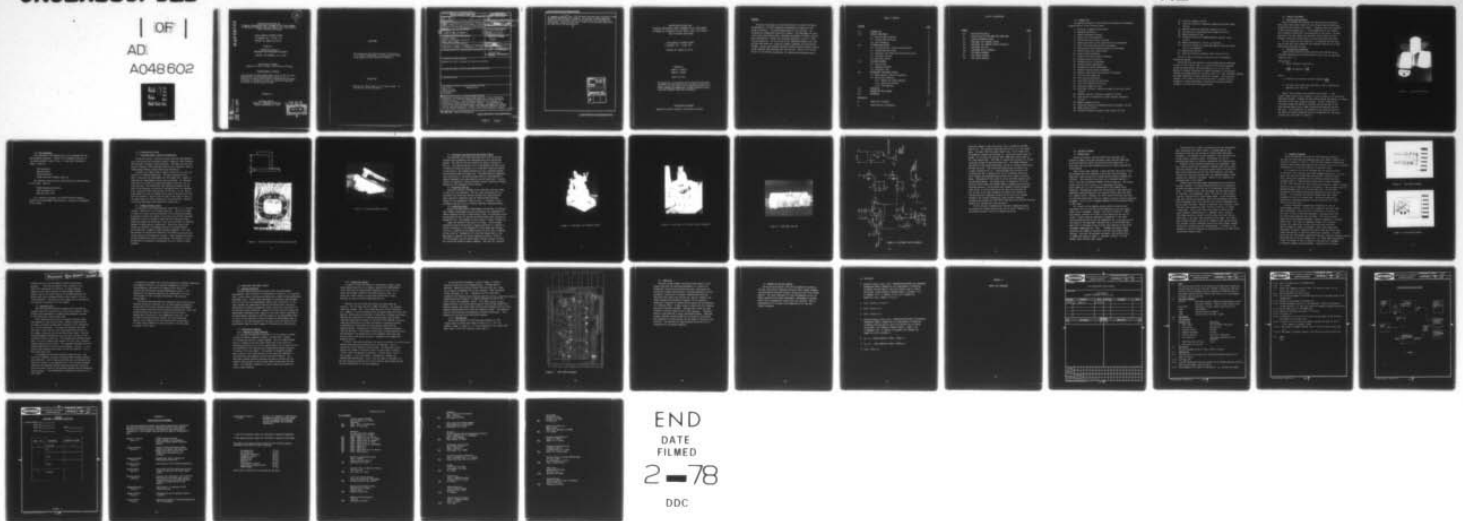
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MANUFACTURING METHODS AND TECHNOLOGY ENGINEERING (MM AND TE) PR--ETC(U)  
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MANUFACTURING METHODS AND  
TECHNOLOGY ENGINEERING (MM&TE) PROGRAM FOR THE ESTABLISHMENT  
OF PRODUCTION TECHNIQUES FOR HIGH DENSITY THICK FILM CIRCUITS  
USED IN CRYSTAL OSCILLATORS

THIRD QUARTERLY PROGRESS REPORT  
28 FEBRUARY 1977 - 29 MAY 1977  
CONTRACT NO. DAAB07-76-C-8119

PLACED BY

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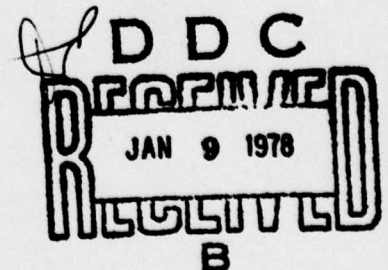
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PREPARED BY

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REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER (6) <i>Final</i>	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER (9)
4. TITLE (and Subtitle) Manufacturing Methods and Technology Engineering (MMTE) Program for the Establishment of Production Techniques for High Density Thick Film Circuits, <i>Used in Crystal Oscillators.</i>		5. TYPE OF REPORT & PERIOD COVERED Quarterly progress report. No. 3 28 Feb 1977 - 29 May 1977
6. AUTHOR(s) (19) C.T./MARTIN C.G./MORRIS		7. PERFORMING ORG. REPORT NUMBER
8. CONTRACT OR GRANT NUMBER(s) (15) DAAB 7-76-C-8119 ✓		9. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 2769767
10. PERFORMING ORGANIZATION NAME AND ADDRESS Raytheon Company Industrial Components Operation Quincy, Mass. 02169 ✓		11. REPORT DATE (12) 9 Sep 1977
12. CONTROLLING OFFICE NAME AND ADDRESS Production Division, Procurement and Production Directorate, USAECOM, Ft. Monmouth, N.J. 07703		13. NUMBER OF PAGES 39 (12) 43 p.
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)		15. SECURITY CLASS. (of this report) Unclassified
15a. DECLASSIFICATION/DOWNGRADING SCHEDULE		
16. DISTRIBUTION STATEMENT (of this Report) Approved for public release; Distribution unlimited		
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)		
18. SUPPLEMENTARY NOTES		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number) Thick film Manufacturing Hybrid Circuits Microelectronics Oscillators		
20. ABSTRACT (Continue on reverse side if necessary and identify by block number) Production techniques are being established for a thick film hybrid microelectronic 17-22 MHz temperature-compensated, voltage-controlled crystal oscillator. In the engineering phase of this program, the following was accomplished during this quarter: the procurement of microcircuit parts and bonding tools, continued procurement of hermetic sealing parts and materials, further test procedure generation, as well as test fixture fabrication. As part of the 10-lot substrate assembly		

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20. Abstract (cont'd) task, TCFG and VCXO substrates were passively trimmed, assembled, and functionally trimmed. Because many problems developed during substrate assembly, hybrid layout redesigns were undertaken for both hybrids. Details of this work, as well as the problems encountered, are reported and documented herein.



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28 FEBRUARY 1977 - 29 MAY 1977

CONTRACT NO. DAAB07-76-C-8119

PREPARED BY  
CHARLES T. MARTIN  
CHARLES G. MORRIS

OBJECT OF STUDY

The objectives of the program are to establish production techniques for high density thick film hybrid microcirucits used in crystal oscillators and to produce quantities of a 20 MHz temperature-compensated, voltage-controlled crystal oscillator (TCVCXO) using those techniques.

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## ABSTRACT

Production techniques are being established for a thick film hybrid microelectronic 17-22 MHz temperature-compensated, voltage-controlled crystal oscillator. In the engineering phase of this program, the following was accomplished during this quarter: the procurement of micro-circuit parts and bonding tools, continued procurement of hermetic sealing parts and materials, further test procedure generation, as well as test fixture fabrication. As part of the 10-lot substrate assembly task, TCFG and VCXO substrates were passively trimmed, assembled, and functionally trimmed. Because many problems developed during substrate assembly, hybrid layout redesigns were undertaken for both hybrids. Details of this work, as well as the problems encountered, are reported and documented herein.

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## 1.0 INTRODUCTION

The engineering phase of this manufacturing methods and technology program consists of the following tasks:

1. Electrical breadboard construction
2. Breadboard evaluation
3. Module configuration design
4. Process flow plan generation
5. Hybrid microcircuit parts selection
6. Hybrid microcircuit parts and bonding tools procurement
7. Thick film processing materials procurement
8. Potting shells and encapsulant materials procurement
9. Hybrid microcircuit layout design
10. Layout artwork generation
11. Thick film printing screen procurement
12. Assembly drawing generation
13. Assembly materials procurement
14. Assembly process development
15. Encapsulation process development
16. Hermetic sealing process development
17. Hermetic sealing parts and materials procurement
18. Test flow plan generation
19. Test procedure generation
20. Text fixture design and fabrication
21. Thick film substrate fabrication
22. Substrate assembly (10-lot)
23. Electrical testing of substrate assemblies (pre-seal tests) (10-lot)
24. Hermetic sealing of substrate assemblies (10-lot)
25. Leak testing of hermetically sealed substrate assemblies (10-lot)
26. Module assembly (10-lot)
27. Electrical testing of assembled modules (pre-aging) (10-lot)
28. Module aging (10-lot)
29. Electrical testing of modules (final tests) (10 lot)

30. Substrate assembly (15-lot)
31. Electrical testing of substrate assemblies (pre-seal tests) (15-lot)
32. Hermetic sealing of substrate assemblies (15-lot)
33. Leak testing of sealed substrate assemblies (15-lot)
34. Module assembly (15-lot)
35. Electrical testing of assembled modules (pre-pot tests) (15-lot)
36. Module encapsulation (15-lot, as required)
37. Electrical testing of encapsulated modules (post-pot tests) (15-lot, as required).
38. Module aging (15-lot)
39. Electrical testing of modules (final tests) (15-lot)

The 10-lot and 15-lot refers to the two lots of deliverable engineering samples.

During the first two quarters of this program work was performed on tasks 1-13 and 16-22, with 1-5, 7 and 9-13 having been completed. During the third quarter, work continued on 6, 8, 17, and 19-22. Because of problems encountered in substrate assembly, a microcircuit redesign has become necessary; therefore, tasks 9-11, once considered complete, have been reactivated for both microcircuit designs. For discussion purposes in this report, the third quarter work is grouped into four categories: process development, fixturing and tooling, substrate assembly, and microcircuit and module design.

## 2.0 PROCESS DEVELOPMENT

### 2.1 Parallel Seal Soldering

Gold-tin preforms were obtained for seam soldering experiments. After some nickel-plated covers were gold plated, these preforms were aligned and spot-welded to the covers. Soldering tests were conducted at Solid State Equipment Corp. Visual examination of the soldered parts indicated inconsistent flow and wetting of the solder. Isolated portions of the seam looked very good while other portions did not. Because of the poorly wetted areas, the parts exhibited gross leaks.

All the reasons are not known, but it is suspected that the parts may not have been clean enough, and more thorough cleaning will be done before future attempts are made.

### 2.2 Potting Shell Evaluation

Sample potting shells have been received and inspected and the following discrepancies have been observed, relative to the specified dimensions [Ref. 1].

Potting Shell:

- 1) Overall length was specified as

$$\frac{1.366}{1.357} \text{ and measured } \frac{1.371}{1.366} .$$

Cover:

- 1) Thickness over ejection pad marks measured  $\frac{.0325}{.0275}$
- 2) The basic radius which was specified as  $.500 \pm .0015$  inch was measured to be .503 inch.

None of these problems are considered to be severe. If the overall length proves to be a problem, it can be ground to fall within the specified tolerance. Probably the most severe problem encountered is a large yield loss in the cover caused by breakage. The wall thickness is very small between the substrate clearance slot and the edge of the cover, and many parts break at that location while being ejected from the mold. This problem will be corrected in any future revision of the tooling or before production tooling is authorized. The fabricated potting shells are shown in figure 2-1.

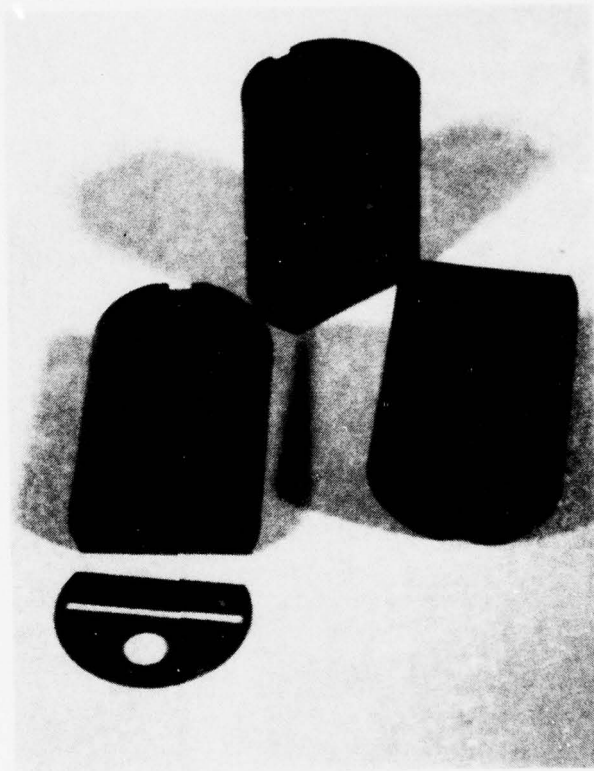


FIGURE 2-1 TCVCXO POTTING SHELLS

### 2.3 Test Procedures

Work continued on the preparation of test procedures for use during module production. Several of the documents outlined in the second quarterly report [ Ref. 2 ] have been finished and typed. These are:

- . TCFG Functional
- . VCXO Functional
- . TCVCXO Functional
- . TCVCXO Transient Frequency Stability

The remaining electrical test specifications are being drafted at this time. They are:

- . TCVCXO Temperature Stability
- . TCFG Functional Trim
- . VCXO Functional Trim

For illustration purposes, the TCVCXO Transient Frequency Stability Test Requirement Specification is included in the Appendix of this report.

### 3.0 FIXTURING AND TOOLING

#### 3.1 Trim Probe Cards - Passive and Functional

During this quarter, fixed point probe cards were fabricated for use in the passive and functional resistor trimming of TCFG substrates and functional trimming of VCXO substrates. The probe cards for the passive trimming of VCXO substrates were not built, because a VCXO re-design became imminent, making these cards obsolescent.

A drawing of a sample probe is shown in figure 3-1 as well as a picture of a completed probe card. The second quarterly report, [Ref. 3] describes the requirements for this probe card. Figure 3-1 shows that all requirements are met with this design. As indicated, the blade of the probe drops down approximately 0.65 inch from its lower top edge. The probe needle then extends horizontally to the point to be addressed, and the end of the needle drops the remaining 0.15", giving the total required drop of 0.80 inch. In this way the probe needle can clear the highest corral used (0.140") and still contact the substrate. Both the vertical drop of the blade and that of the probe needle are custom designed for this application, resulting in the long procurement time required for these cards.

#### 3.2 Trimming Holding Fixture

As discussed in the second quarterly report [Ref. 4] an "elevator" fixture is required for all trimming operations. This fixture shown in figure 3-2 allows corralled substrates to be inserted and removed. By pushing or pulling the handle on the side of the fixture, the upper platform is raised or lowered in order that the fixed point probes either may contact the substrate or clear the corral when the substrate assembly is being removed, respectively. During this quarter, the fixture was modified to incorporate the use of an edge connector during functional trimming of VCXO substrate assemblies. This step was necessary as spurious oscillations on the output occurred with the initial set-up and dictated more intimate contact between the crystal and VCXO assembly than probes could provide. The fixture will also be modified to incorporate a thermocouple to aid in TCFG functional trimming.

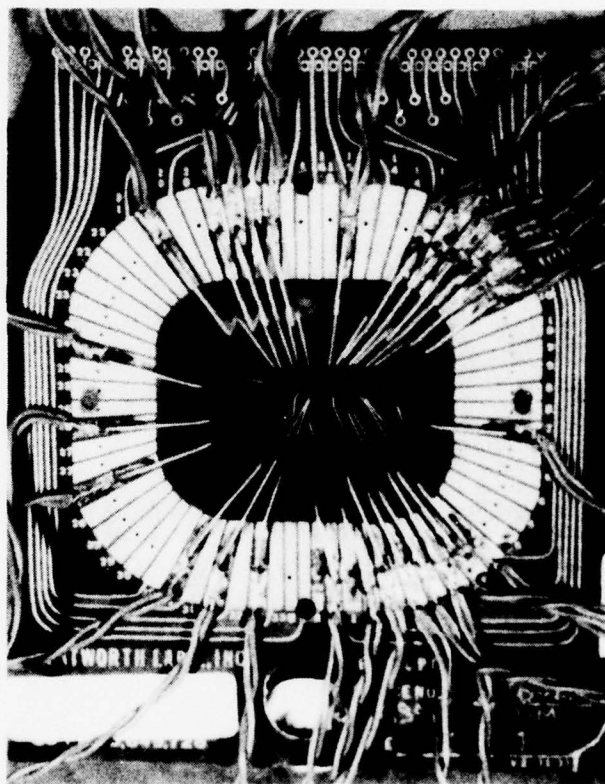
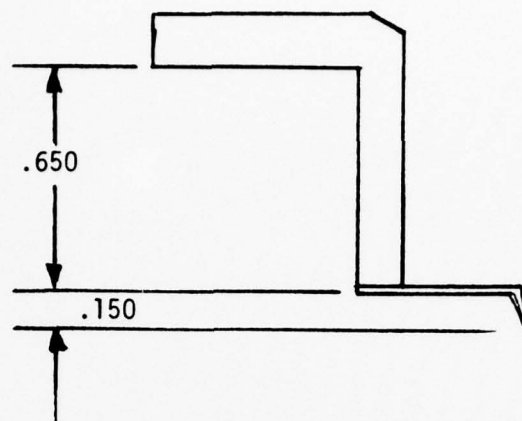


FIGURE 3-1 PASSIVE RESISTOR TRIM PROBE AND PROBE CARD

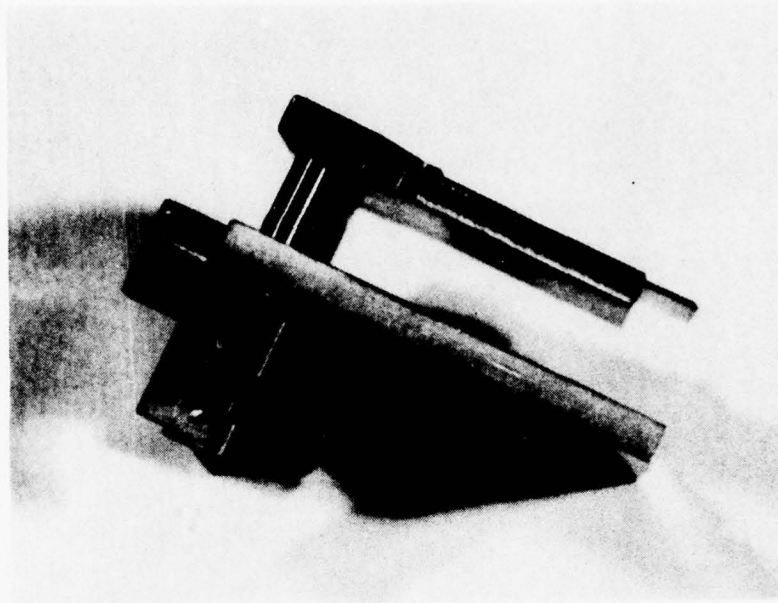


FIGURE 3-2 ELEVATOR TRIMMING FIXTURE

### 3.3 Functional Test Probe Card and Holding Fixture

The functional test fixture and probe card, used for testing unsealed hybrid assemblies were fabricated and set up during this quarter. Two views of this test station are shown in figures 3-3 and 3-4. The station consists of (1) a microprober with optics and a fixed point probe card holder, (2) a fixed point probe card similar to those used in the trimming operation and (3) a substrate holding fixture mounted under the probe card. The unsealed hybrid assemblies rest side-by-side in the holding fixture and are interconnected to external equipment by an edge connector and the probe card. The substrates are removed by lifting the probe ring and slipping the holding fixture out from underneath the microprober.

### 3.4 Functional Test Box

During this quarter, assembly of the functional test box, shown in figure 3-5, was completed. This box, when interfaced with the functional test probe card station, provides the interfacing and loads required to completely test the TCFG and VCXO substrates (except for the temperature stability test). A connector is also provided on the box for use in testing completely assembled modules.

### 3.5 Electronic Switch

Because the ECOM Technical Requirements SCS-483 [Ref. 5] dictates that frequency measurements be made continuously over temperature at center frequency and each of the deviation limits, an electronic switch was designed and built to provide the TCVCXO analog input required to accomplish this. The schematic of this circuit is shown in figure 3-6.

Inputs are applied to the switch as follows. The DC voltage required to obtain the positive or negative deviation is applied to the DC IN terminals, a low frequency TTL level square wave (around 0.05 Hz) is connected to the CLOCK IN jack, and five volts is applied to the circuitry. Assuming all J-K flip flop outputs begin at low when power is applied, the circuit operates as follows. With all flip flop outputs low, the analog input is pulled to ground by relay K2, driving the TCVCXO to center frequency. When the first positive

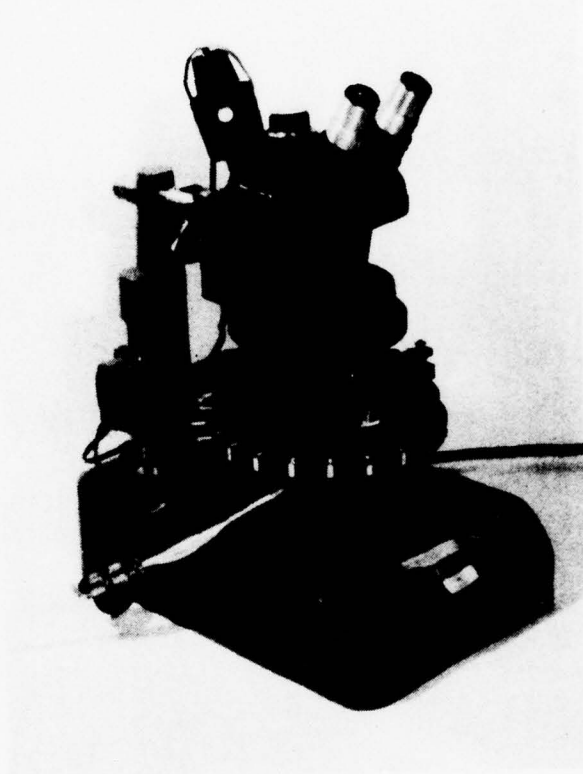


FIGURE 3-3 FUNCTIONAL TEST PROBING STATION

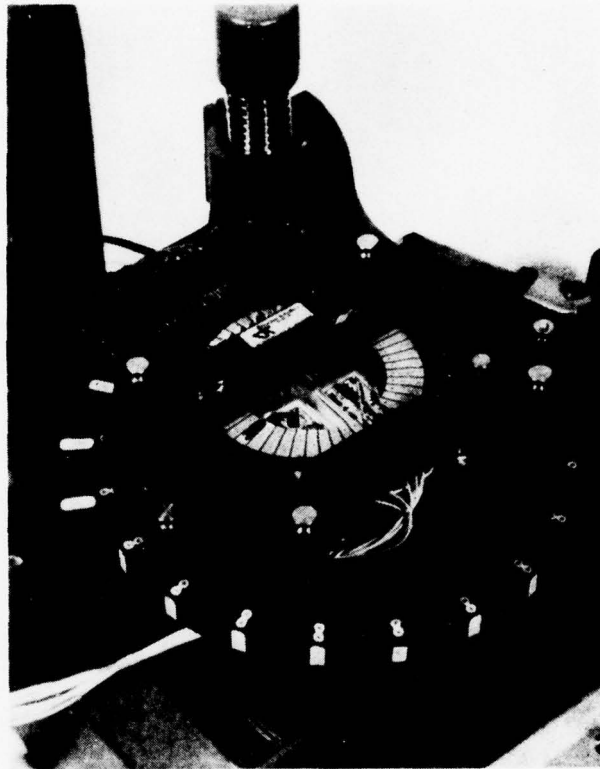


FIGURE 3-4 FUNCTIONAL TEST PROBING STATION (CLOSE-UP)

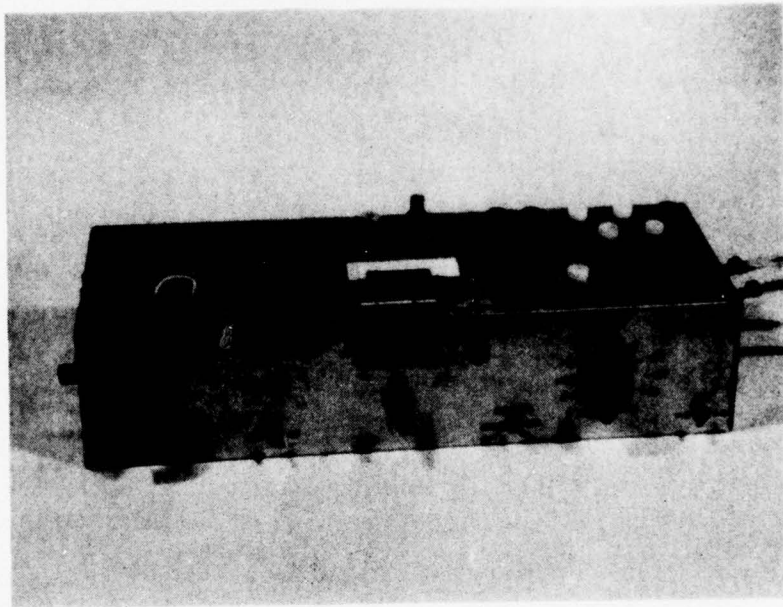
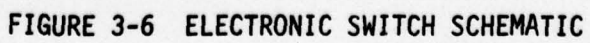


FIGURE 3-5 FUNCTIONAL TEST BOX



transition appears on the clock pulse, and is inverted by the NAND gate U1 (1). This negative transition clocks U2 (1) to a high output state. The other flip-flop output remains low. U2 (1) feeds relay K2 through an inverter and activates it, pulling the analog input off ground. U2 (1) and U2 (2) outputs feed a NAND gate, whose output at this time remains high. This high is inverted and activates K1, placing a positive voltage on the analog input line. The TCVCX0 frequency then shifts to the positive deviation, and the X-Y plotter needle moves, but does not print. The clock pulse negative edge now occurs, and is again inverted by U1 (1). A positive edge has no effect on the J-K flip-flop, but is inverted by U1 (3) to a negative transition, which triggers the monostable multivibrator U4 to output a positive pulse. The duration of this pulse is set by the three capacitors and the 50K potentiometer. The output pulse is inverted by U1 (4) and drives Q1, which sends the recorder needle a command to print during the pulse duration. By continuing this reasoning through subsequent clock pulses, it can be seen that on the next clock pulse, U2 (1) will go low, U2 (2) high, grounding the analog input through K2. The next pulse will generate a high on U2 (1) and U2 (2), thereby driving U1 (2) low, thus releasing K1, and allowing a negative voltage on the analog line. The fourth clock pulse will set both flip-flop outputs low, starting the cycle over again.

If this circuit is operated over the entire temperature range, the plotter will produce three curves; one at center frequency, one at positive deviation, and one at negative deviation.

#### 4.0 SUBSTRATE ASSEMBLY

##### 4.1 Passive Trim

During this quarter, TCFG and VCXO 10-lot substrates were passively trimmed, using both the manual probe technique (described in the 2nd quarterly report) and the fixed point probe cards. In both cases, the trims were accomplished, but not without encountering a few problems.

After corrals were attached, it was noted that their glass fillets had extended toward the substrate interior more than anticipated. In some cases, glass had partially covered resistors, making trimming very difficult. This occurred as the result of a tolerance problem in corral and their associated alignment fixture dimensions. The ceramic corrals could be built to only a  $\pm 1\%$  dimensional tolerance, which equates to a  $\pm 12$  mil tolerance band in the longest corral dimension. Although the corrals were lot-consistent, their particular dimensions caused problems with our substrate design, which was based on a nominal corral. Secondly, our corral attach fixturing, described in a previous report [Ref. 6], is not capable of precise corral-to-substrate alignment. This  $\pm 2$ -3 mil alignment problem also had an adverse effect in some areas.

As a result of this problem, several possible solutions were considered. The first and most obvious approach was passive trimming before corral attachment. However, since corral attach is a  $500^{\circ}\text{C}$  plus process, resistors will shift in value because of the heat involved. A small study was undertaken to determine if this shift could be predicted and, in turn, be compensated for in the passive trim. The results of the experiment indicated that a 4-5% consistent downward shift in resistance values occurred after exposure to the corral attachment temperature and time. Although the results looked promising, on a number of occasions a resistor would behave unpredictably. With over 100 resistors per module, this would not have to happen very often to render a substrate useless. For this reason, other solutions were sought.

The possibility of tighter toleranced corrals was investigated. After discussion with several vendors, it became apparent that machining corrals was the only way to tighten their dimensional tolerances. The problem with this approach is that the possibility of the ceramic cracking is great. In addition, the cost of machining would make this solution uneconomical for production use.

Redesign of both substrate layouts was also considered. There was a serious question as to whether a redesign could really accomplish the objective after taking into account worst case corral and glass fillet dimensions and the high circuit density. With some relaxation of the design ground-rules, the redesign became a viable solution and, therefore, was begun. Details of this redesign are presented later in this report.

Another design-related problem became apparent during passive resistor trimming. To enhance manufacturability of the substrates, an effort was made to avoid the use of an additional resistor paste blend. To accomplish this, some one megohm resistors were designed as 'top hats', using 300K  $\Omega/\square$  paste. By nature of their design, 'top hat' resistors have a high trimming range. It was anticipated that these resistors, as designed, would fire considerably lower than their one megohm final value, and that this could be compensated for by the large trim range. Because of substrate size limitations, these 'top hats' were necessarily small, having a little as .01" widths in some cases. Due to their small size, these resistors did not screen properly, yielding more of a 'sombrero' than a 'top hat'. This effect drove the resistor's initial value even lower than expected and, at the same time, reduced the trim range. As a result, some of these resistors could not be trimmed to their desired values. This problem is being eliminated by using four paste blends, thereby allowing for optimized resistor configurations. In essence, it was necessary to sacrifice some ease of manufacturability, in order to gain the desired trimming results.

#### 4.2 Component Assembly

During this quarter, thirteen (13) TCFG substrate assemblies and eight (8) VCXO substrate assemblies were built. Sample assemblies are pictured in figures 4-1 and 4-2. While the TCFG component assembly went smoothly, VCXO assembly posed many serious problems, enough so as to warrant consideration of a substrate redesign on that basis alone.

As in passive trim, corral tolerances and the associated shift in the glass fillet location caused VCXO assembly difficulties. In a few areas, wire bond and die bond pads were partially covered by corral glass, making chip attachment and wire bonding a tedious and time consuming process. These problems mainly occurred around components U6, CR11, CR12, and CR14. The corral height also generated assembly problems. Because of corral dimensions and circuit density, some components had to be mounted extremely close to the inside corral wall, so close that conventional die bonding and beam lead bonding tools would not clear the wall. To circumvent this problem, bonding tools were ground extremely thin for use in these areas. Q4 and CR14 were two exceptionally troublesome components to mount because of their proximity to the corral wall.

Several alternative solutions were considered in light of these assembly problems. First of all, changes in the corral shape were investigated. Since the crux of the problem is proximity of the corral to chip or beam lead components, a narrower corral with the same outside dimensions was considered. This would free more space near the troublesome components, thereby accommodating a standard bonding tool. This idea was abandoned, however, for structural reasons; the large height to width ratio would make the corral weak and subject to cracks or breakage. Other corral shapes were considered, including a tapered corral whose inside wall would slope inward from the top, to allow for bonding tool clearance. A shorter corral was also investigated, wherein the necessary component clearance would be maintained thru the use of a domed cover. All these ideas were rejected either for reasons of cost or amount of time required to implement or potential hermetic sealing problems. Continuing to use special

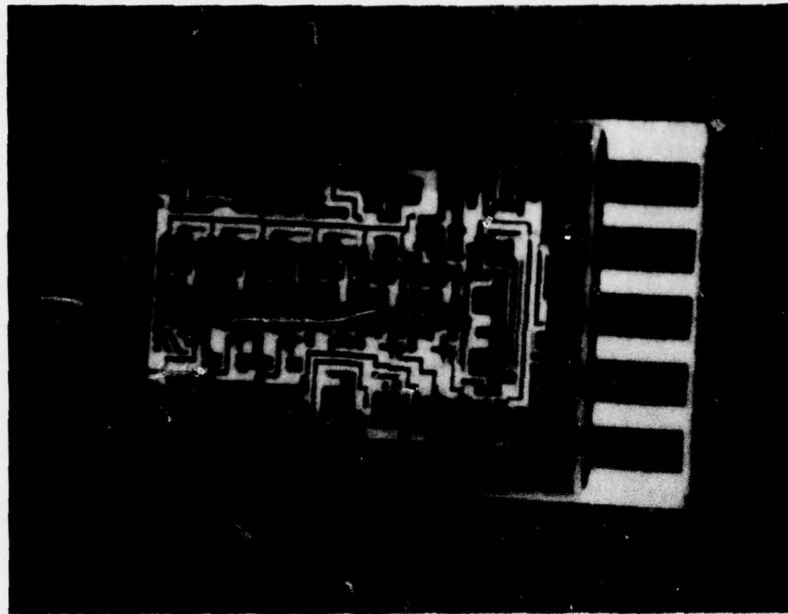


FIGURE 4-1 TCFG HYBRID ASSEMBLY

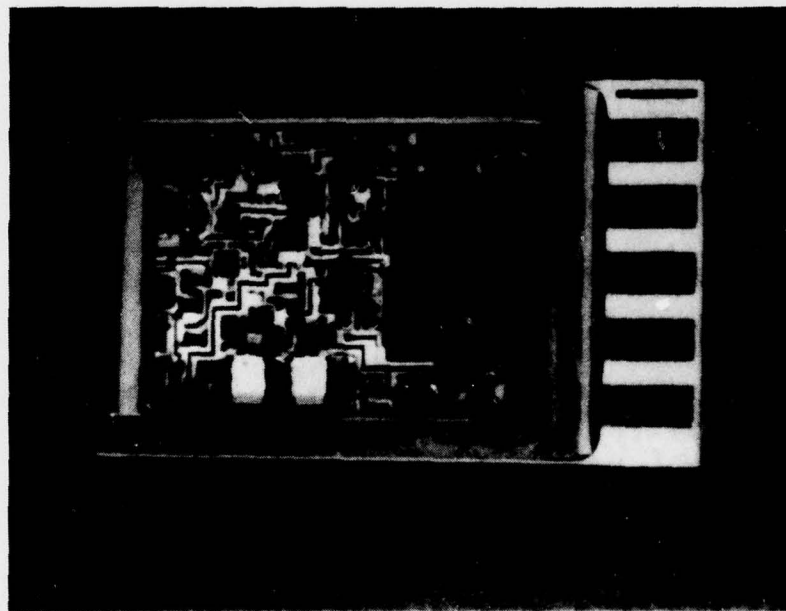


FIGURE 4-2 VCXO HYBRID ASSEMBLY

bonding tools was also considered, but this was dismissed outright. Even with the special tools, assembly of the VCXO 10-lot substrates was difficult. A layout redesign seemed the only viable solution to these assembly problems. However, due to the circuit density of the VCXO substrate, the design could not be improved without a major change in the design groundrules. The details of this change and its implications are discussed in section 5.2 of this report.

#### 4.3 Functional Trim

Both TCFG and VCXO substrate assemblies were functionally trimmed during this quarter for use in the 10-lot modules. Minor problems were encountered in trimming TCFG assemblies, but most of the difficulties involved VCXO trims.

Noise, generated by the laser and machine lighting caused some problems in high accuracy trims. Before corrective action was taken, voltmeter readings would fluctuate 1 mV or more, making a  $\pm 1$  mV trim impossible. To correct this problem, two steps were taken. After the laser was aligned beside the resistor to be trimmed, lights were put out and the trim was begun. When the reading approached the desired value, the laser was shut off and the meter allowed to stabilize. This procedure was repeated several times per trim, trimming small amounts at a time, until the meter reading stabilized within range. This procedure decreased the noise problem significantly, but was slow and tedious. The setup is presently being evaluated with respect to noise elimination, so as to facilitate these trims.

In attempting to trim VCXO substrate assemblies to a given oscillator frequency, spurious oscillations made frequency measurements difficult. Since these oscillations had not occurred during functional testing, it was assumed to be a laser fixturing problem. Therefore, the substrate holding fixture was modified in order to bring the crystal closer to the substrate assembly and the problem was thus eliminated. This modification is described in section 3.2 of this report.

Calibrating by trimming TCFG substrate assemblies to ambient temperature was somewhat difficult as the measured temperature of the substrate wandered a few tenths of a degree Celsius due to air currents and intermittent substrate-thermocouple contact. This problem will be reduced by mounting the thermocouple in the substrate holder so that it touches the bottom of the substrate being trimmed.

Various problems associated with substrate layout design were encountered during the functional trim. On TCFG substrate assemblies, resistor R57 did not have sufficient range to permit the trimming of the voltage across R57 to within specification.[See Ref.7] Also, R57 and R48 resistors were partially covered with corral glass, causing some difficulties in the compensating curve trim. R75 and R80 on the VCX0 substrate assembly also had insufficient range to trim frequency shift into specification in some cases. All these layout problems are being corrected in the new design discussed in this report.

## 5.0 MICROCIRCUIT AND MODULE DESIGN

### 5.1 Moisture Protection

The ECOM TCVCXO specification requires that the potentiometer be accessible after the module is encapsulated. In addition, it is required that a certain amount of moisture protection be provided to the potentiometer adjustment screw. To meet these requirements a bushing has been designed which will encircle the potentiometer adjust screw, enclosing it in the region between the potentiometer body and the potting shell inner wall. The bushing is internally threaded to accept a nylon set screw which will provide the moisture protection. Removal of the set screw will expose the potentiometer adjustment screw. Because of the loose factory tolerances of the potentiometer adjustment screw with respect to the potentiometer body, a fixture will be required to align and secure the potentiometer body to the module. A silicone elastomer will be used to seal the bushing to the potentiometer body to prevent leakage of the encapsulant during potting.

### 5.2 Microcircuit Redesign

#### 5.2.1 Reasons for Layout Redesign

As outlined and explained in Section 4.0 of this report, problems in passive trimming, component assembly, and functional trimming all dictated the need for a layout redesign. Passive trimming showed that (1) a number of resistors were covered with corral glass and, therefore, were difficult to trim and were unstable and (2) some resistors had insufficient trim range due to the fabrication problem discussed in Section 4.1 of this report. The problems in component assembly were a result of the close proximity of wire bonds and components to the corral wall and indirectly of the high circuit density. The functional trimming problems indicated the need to increase the trim range of some resistors as well as move others farther away from the corral. As indicated in Section 4.0, each of these areas alone dictated a layout redesign.

### 5.2.2. Ground Rule Changes

In order to insure the success of the redesign, several layout design ground rules had to be changed, some requiring ECOM approval. First, both TCFG and VCXO substrate assemblies will use four resistor paste blends instead of the three previously used. By doing this, better control of resistor-as-fired values is made possible, at some sacrifice of manufacturing cost.

Secondly, the use of beam lead devices has been abandoned entirely. This has been done for a number of reasons. The original intent was to make wide use of beam lead chips in the TC/CXO module. However, it was discovered early in the program that only two of the required device types were available in beam leads. Although the original 100% goal was impossible, the hybrids were designed using the beam lead devices that were available. At the time of the redesign, it was decided that continuing to use beam lead placed an unnecessary burden on manufacture of the hybrids (an extra process step) with few benefits derived. Additionally, a reliability consideration entered into this decision. Since solder must be used to attach capacitors onto the VCXO hybrid, the possibility of flux entrapment under beam lead devices exists, even though the hybrid assemblies are cleaned after capacitor attach.

Criteria have been established for corral-to-chip and for corral-to-wire bond pad distances and are being used in the redesign. Also, a 'worst case' corral approach is being taken. The dimensions of the smallest and largest in tolerance corral are being used to define a 'no-man's land' for devices or resistors. A 0.015" glass fillet is also assumed in this calculation. Although this reduces the working space considerably, much of the lost space is recovered on the TCFG substrate through the use of four resistor paste blends and the resultant optimization of resistor geometries.

On the VCXO hybrid assembly, a drastic change in concept is required to make the circuit manufacturable. Although devices obviously needed to be placed farther from the corral wall, there was no room to accommodate this on the substrate. After discussion of many solutions, it was decided to use the large space occupied by the flatpack crystal mounting pad for circuitry, since the crystal is presently outside the hybrid. A logical candidate for use of this area is the 9 volt regulator circuit. Thus, when flatpack crystals become available, this entire section may be lifted out and placed into a separate package, the crystal moved into the hybrid assembly and the 9 volt regulator mounted where the crystal was formerly located. The regulator could be interconnected using presently available outside pads. This approach will be used on the VCXO hybrid redesign.

#### 5.2.3 TCFG Redesign

During this quarter, the TCFG substrate assembly was redesigned using the ground rules noted in Section 5.2.2. This redesign is shown in Figure 5.1. It can be compared to the original TCFG layout shown in the first quarterly report [Ref. 8].

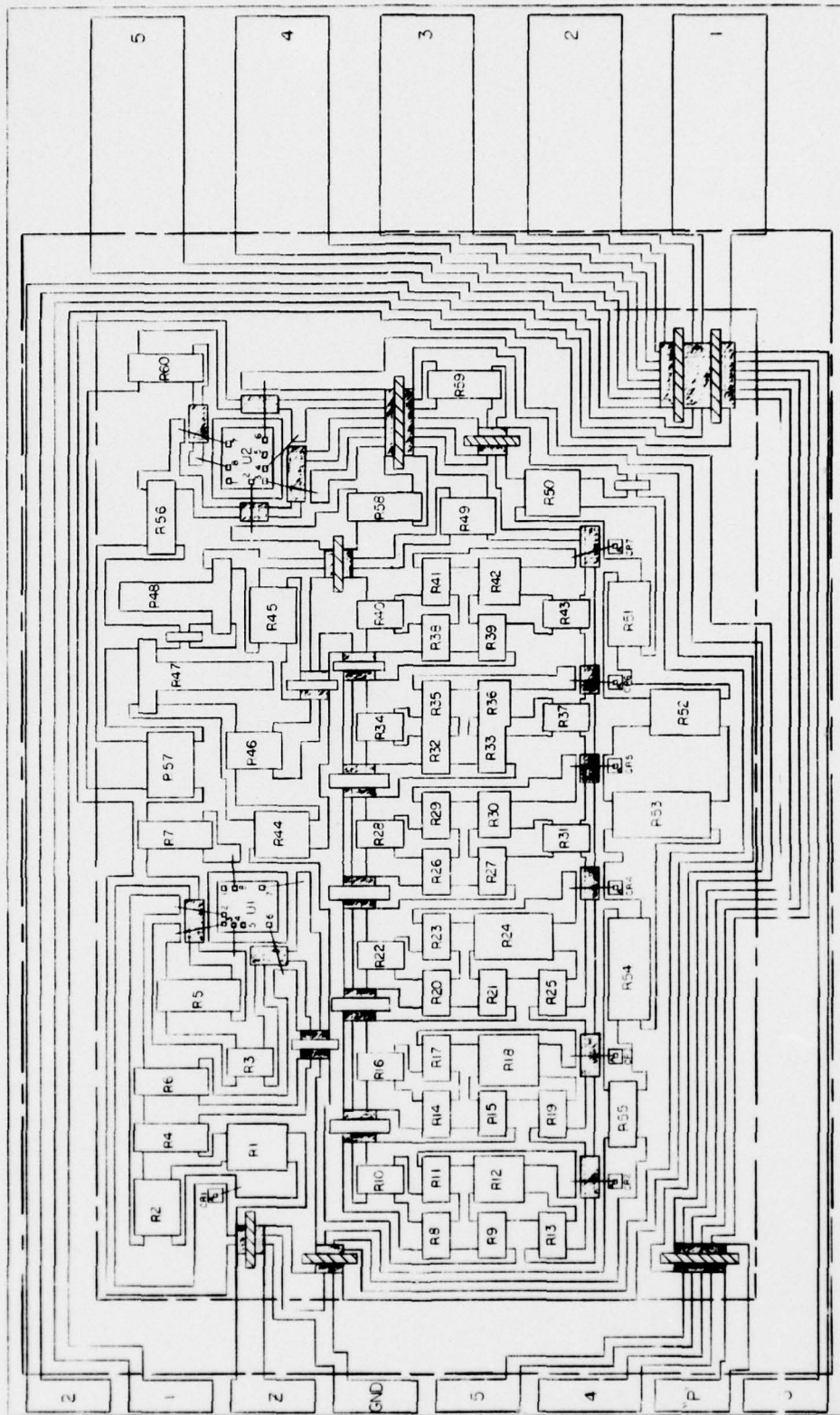


FIGURE 5-1 TCFG LAYOUT REDESIGN

## 6.0 CONCLUSION

The major accomplishments during the third quarter of this program have been the continued development of a process for hermetically sealing the hybrid microcircuits, fabrication and evaluation of sample potting shells, continued generation of test procedures, fabrication of resistor trimming probe cards and functional test probe cards and test box, passive trimming, component assembly and functional trimming of 10 lot substrate assemblies, evaluation of present hybrid layouts and the beginning of a redesign effort. To date, areas of concern are still hermetic sealing and substrate assembly. Although some success has been achieved in sealing, there are still some concerns; therefore, parallel seam soldering is being investigated further. Substrate assembly problems include trimability of resistors, positioning and attachment of active devices, and the range of functional trim resistors. The solutions to these problems are and will be incorporated into the layout redesigns.

#### 7.0 PROGRAM FOR THE NEXT QUARTER

During the next quarter, work will be completed on hermetic sealing, leak testing, substrate electrical tests, module assembly, pre-aging module functional testing, and aging of the 10-lot TCVCX0 modules. The layout redesigns will also be completed, as will be artwork generation and screen procurement. Development of potting shells and an encapsulation process will also continue. Work on documentation will continue, with completion of all test procedures scheduled.

## 8.0 REFERENCES

1. Raytheon Company, Quincy, Mass., MANUFACTURING METHODS AND TECHNOLOGY ENGINEERING (MM&TE) PROGRAM FOR THE ESTABLISHMENT OF PRODUCTION TECHNIQUES FOR HIGH DENSITY THICK FILM CIRCUITS USED IN CRYSTAL OSCILLATORS, SECOND QUARTERLY PROGRESS REPORT, 22 NOVEMBER 1976 - 27 FEBRUARY 1977, C.T. MARTIN, 12 JULY 1977 (CONTRACT NO. DAAB07-76-C-8119, FIGURES 3-1 and 3-2.
2. Ibid., Sections 3.3 and 3.4
3. Ibid., Section 4.2.1
4. Ibid., Section 4.2.1
5. Raytheon Company, Quincy, Mass., MANUFACTURING METHODS AND TECHNOLOGY ENGINEERING (MM&TE) PROGRAM FOR THE ESTABLISHMENT OF PRODUCTION TECHNIQUES FOR HIGH DENSITY THICK FILM CIRCUITS USED IN CRYSTAL OSCILLATORS, FIRST QUARTERLY PROGRESS REPORT, 6 AUGUST 1976 - 21 NOVEMBER 1976, C.T. MARTIN, 30 DECEMBER 1976 (CONTRACT NO. DAAB07-76-C-8119), APPENDIX A.
6. Op. cit., SECOND QUARTERLY REPORT, FIGURE 5-4.
7. Op. cit., FIRST QUARTERLY REPORT, APPENDIX B.
8. Ibid., Figure 16

APPENDIX A

SAMPLE TEST PROCEDURE



## 1.0 SCOPE

This specification applies to the testing of the temperature-compensated voltage-controlled crystal oscillator (TCVCXO) to demonstrate compliance with the Transient Frequency Stability requirement of USAECOM Technical Requirements SCS-483, dated 17 January 1975, Section 3.13, and amendment 3 thereto, dated 14 June 1976.

## 2.0 APPLICABLE DOCUMENTS

SCS-483	Oscillator, Crystal, Temperature-Compensated, Voltage-Controlled (TCVCXO), 17 MHz to 22 MHz, Hermetic Seal.
MIL-0-55310	Oscillators, Crystal, General Specification for
31380	TCVCXO Module
31383	TCVCXO Electrical Schematic
31382	Electrical Test Flow Plan, TCVCXO

## 3.0 REQUIREMENTS

### 3.1 TEST EQUIPMENT

<u>Equipment Item</u>	<u>Description</u>
1. Power Supply	Harrison 855B or equivalent
2. Oscilloscope	Tektronix 547
3. Frequency Counter	HP 5360
4. Keyboard Programmer	HP 5375
5. Function Generator	Exact 301 or equivalent
6. Pulse Generator	Interstate Instruments PG-2 or equivalent
7. TCVCXO Functional Test Box	31366
8. Patch cords, as required	

### 3.2 TEST SET-UP

The test equipment set-up will be as shown in figure 1.

### 3.3 TURN ON TEST

- 3.3.1 Test data shall be recorded on the Transient Frequency Stability form shown in figure 2.
- 3.3.2 Turn power off.
- 3.3.3 Plug the TCVCXO module into the connector on the TCVCXO Functional Test Box, and place the thermal shield in place.
- 3.3.4 Switch ANALOG to OV, Control to DIG, IFBK to -  $\Delta$  , and Turn On to Norm,

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- 3.3.5 Place the 5360 counter in the MODULE mode.
- 3.3.6 Turn on power.
- 3.3.7 Observe the frequency and verify that it is stable to within  $\pm 0.2$  Hz. Record this value as F initial.
- 3.3.8 Switch TURN-ON to the TEST position.
- 3.3.9 Set the 5375 programmer to the START position and set the 5360 counter to the EXTERNAL mode.
- 3.3.10 Depress the push button on the EXACT 301.
- 3.3.11 The 5375 programmer should be in the PAUSE mode. RECALL the contents of storage registers a, b, and c and record the frequency displayed respectively.
- 3.3.12 Set the 5360 counter to the MODULE mode.
- 3.3.13 Observe the frequency and record it as F final.
- 3.3.14 Turn power off.
- 3.3.15 To determine if the results of this test are acceptable, do the following data reduction on the test form.
- 3.3.15.1 Subtract F initial from each frequency recorded and enter the result, in the "change in frequency" column.
- 3.3.15.2 The change in frequency entered in the F initial row must be less than 1 Hz.
- 3.3.15.3 The change in frequency entered in the F100 row must be less than 9 Hz.

4.0 NOTES  
None

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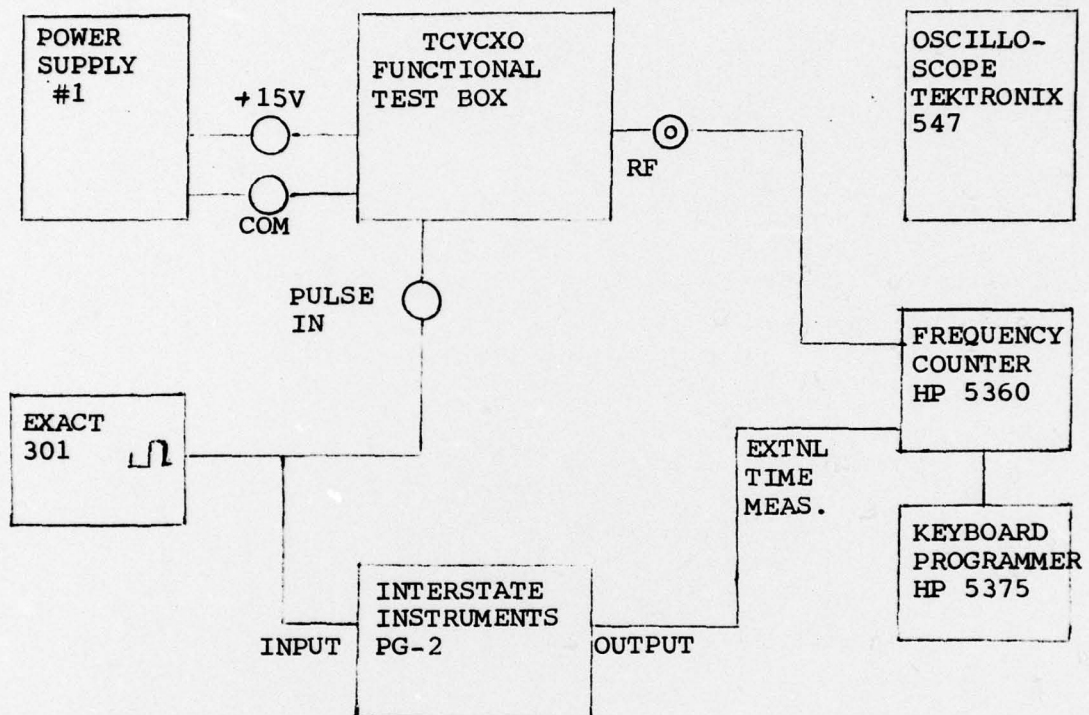
TCVCXO TURN-ON TEST SETUP

FIGURE 1

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TCVCXO  
TRANSIENT FREQUENCY STABILITY

TCVCXO MODULE NO: \_\_\_\_\_

TCFG NO: \_\_\_\_\_

VCXO NO: \_\_\_\_\_

XTAL NO: \_\_\_\_\_

DATE: \_\_\_\_\_

BY: \_\_\_\_\_

TEST NO.	FREQUENCY	CHANGE IN FREQ.
1.	$F_{\text{initial}} =$	0
2.	$F_5 =$	
	$F_{50} =$	
	$F_{100} =$	
3.	$F_{\text{final}} =$	

FIGURE 2

## APPENDIX B

### IDENTIFICATION OF PERSONNEL

The following Raytheon Equipment Development Laboratories professional personnel performed work on this program during the second quarter. The man-hours of work charged to the program by each individual is reported, as is the program, contributions and technical background of each.

Charles T. Martin* (90 hrs.)	TCVCXO Engineering Phase Project Manager; also prepared engineering phase monthly technical reports.
Leland Woodworth* (9 hrs.)	Prepared TCVCXO engineering phase monthly cost reports and supervised production control activity for TCVCXO parts and materials pro- curement.
Stanley Czerepak* (46 hrs.)	Accomplished layout redesign for TCFG hybrid microcircuit.
Richard Colson* (3 hrs.)	Contributed to test procedure generation.
Richard Bemis* (90 hrs.)	Tested TCFG and VCXO hybrid microcircuit assemblies during 10-lot module fabri- cation.
Charles Morris* (290 hrs.)	Prepared test procedures, test fixturing, and resistor-trim probe cards and per- formed passive and functional resistor trimming of substrates for 10-lot modules.
Joseph Malatino** (40 hrs.)	Participated in redesign of TCFG substrate layout.
Thomas Salzer** (8 hrs)	Performed set-up for hermetic sealing of hybrid.
Frank Cheriff (8 hrs.)	Supervised assembly of hybrid microcircuits for 10-lot modules.

Frank Cheriff (cont'd)  
(8 hrs)

B.S.M.E., Sr. Engineer in Microcircuit  
Engineering Section and group leader  
for hybrid assembly and packaging  
process development and prototype  
fabrication.

\* See first quarterly report for individual's technical background.

\*\* See second quarterly report for individual's technical background.

The above-listed personnel were assisted by the following support  
functions at the level of effort indicated:

QC engineering	17 hrs.
QC inspection	21 hrs.
Electrical technician	66 hrs.
Production control	86 hrs.
Manufacturing	60 hrs.
Machine shop	37 hrs.
Drafting	51 hrs.
Environmental testing	28 hrs.
Supervision & administration	22 hrs.
Miscellaneous	16 hrs.

Total level of effort for this quarter was 784 hours.

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